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Remarks

Thorough examination by the Examiner is noted and appreciated.

The Claims have been amended to clarify Applicants disclosed and claimed invention.

Limitations from claims 4 and 5 have been included in claim 1 and the limitations in claim 13 included in claim 12 to more clearly define the invention over the prior art. New claim 21 includes limitations previously included in claims 1 and 12 related to the detailed structure of the wafer lifter.

Support for the amended claims is found in the original claims and/or Specification. No new matter has been entered or new issues requiring further consideration raised.

Claim Rejections under 35 USC 103(a)

1. Claims 1, 3-5, 7-8, 11-13, 15-17, and 19 stand rejected under 35 USC 103(a) as being unpatentable over Ishi et al., (US 5,571,366) in view of Somekh et al. (US 5, 643, 366) or Bors et al. (EP 0276061).

Ishi et al. disclose a plasma processing apparatus whereby the plasma pressure or light emitted from the plasma is monitored

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in-situ and a voltage source for supplying a radiofrequency is controlled in response to the in-situ monitoring (see abstract).

In one embodiment a vertically moveable support mechanism (see col 11, line 32-36; Figure 12, item 76) together with a vertically moveable pusher pin mechanism (item 77) embedded in the electrostatic wafer chuck to remove the wafer from the electrostatic chuck following wafer processing. Ishi et al. does not disclose the structure of the vertically moveable support mechanism other than what is shown in Figure 12.

Ishi et al. does not disclose Applicants claimed and disclosed semiconductor wafer lifter structure. For example, Figure 12, which shows the wafer lifter of Ishi et al., shows a two fingered lifter (item 76) that contact the semiconductor wafer on the process face at the periphery. Ishi et al. does not disclose the claimed structure of Applicants claims semiconductor wafer lifter including a bottom portion having a circular opening on which the semiconductor wafer periphery rests.

Ishi et al. further does not disclose or suggest that an electrical bias is or can be supplied through a semiconductor wafer lifter. Rather in the apparatus of Ishi et al. the semiconductor wafer holder is taught only to be electrically biased through the electrostatic chuck.

Ishi et al. fail to disclose several aspects of Applicants disclosed and claimed invention and the wafer lifter of Ishi et al. operates by a different principal of operation (i.e., touching the semiconductor process face only at two points on the wafer periphery with the two fingered wafer lifter).

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Somekh et al., on the other hand discloses a "C" shaped wafer support (wafer lifter) with a **three fingered contact surface** to raise a semiconductor wafer to contact a susceptor (wafer chuck) (see abstract, col 2, lines 6-18). The wafer lifter (wafer support assembly) is then lowered and moved out of the path of the susceptor (col 2, lines 26-30) is lowered for plasma processing. The purpose of the "C" shaped wafer support is to allow a susceptor arm to move the susceptor holding the wafer downward into a processing position (col 3, lines 1-8).

Bors et al. disclose a plasma chamber for CVD deposition including a manipulator arm and blade (wafer lifter) that transfers a wafer from a cassette in a loading chamber to underneath a wafer chuck located at a top portion of the plasma chamber by rotating horizontally 90 degrees. A **3-arm lifting mechanism** on the blade, each arm having ceramic fingers then lifts the wafer to contact the chuck, similar to Somekh et al.:

"The manipulator arm 68 is rotated by a motor through a 90 DEG angle. The loadlock 64 is opened and the manipulator arm 68 extends carrying the blade 70 with wafer 46 into the center of the deposition chamber 16. **Three lifting arms 72 each having a ceramic finger 74** approximately one-eighth inch in diameter attached to support 71, lift the wafer 46 off the blade and contact the back side of the wafer 46, face down, with the chuck 76. A larger number of ceramic fingers can be used to avoid the necessity of prealigning the wafer to orient the flat, however, **typically 3 fingers are used with prealignment** of the wafers in the cassette."

Neither Somekh et al. or Bors et al. teach a wafer lifter having the same structure and operation of Applicants disclosed and claimed invention including holding the wafer in a face down processing position **during plasma processing** at a top of the

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plasma chamber with an electrical bias supplied to the **semiconductor wafer and the semiconductor wafer lifter.**

Thus, the structure of the wafer support (lifter) of Somekh et al. or Bors et al. is different from both Ishi et al. and Applicants disclosed and claimed invention. The wafer lifter of Somekh et al. or Bors et al. does not hold the wafer at a top of the plasma chamber **during plasma processing**, but rather raises the wafer to contact a susceptor (wafer chuck), which holds the wafer during processing while the wafer lifter is move out of the way of the plasma process. Thus, the wafer lifter of Somekh et al. or Bors et al. works by a different principal of operation compared to Ishi et al. as well as Applicants disclosed and claimed invention. There is no apparent motive for combining the teachings of Ishi et al. with Somekh et al. or Bors et al. For example, holding the wafer at a top portion of the plasma chamber during processing (as shown in Ishi et al.) with the wafer lifter of Somekh et al. or Bors et al. would destroy the principal of operation of the wafer lifter of Somekh et al. or Bors et al., interfering with movement of the susceptor as taught by susceptor as well as interfering with a plasma process such as etching or CVD deposition. Conversely, removing the wafer lifter prior to plasma processing or moving the susceptor downward to avoid the wafer lifter for processing as taught in the operation and structure of the apparatus of Somekh et al. or Bors et al. would destroy and make unworkable the principal of operation of the apparatus of Ishi et al., since the wafer lifter of Ishi et al. holds the wafer in place during processing.

Nevertheless, assuming *arguendo* a proper motive for combining Ishi et al. and Somekh et al. or Bors et al., such combination does not produce Applicants disclosed and claimed

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invention. None of the references, alone or in combination, discloses the structure and operation of Applicants wafer lifter. Moreover none of Ishi et al., Somekh et al. or Bors et al., alone or in combination suggest, disclose or teach supplying an electrical bias to the wafer lifter, or disclose a structure where such would be possible. Applicants suggest that the two fingered structure of Ishi et al. and the three fingered structures of Somekh et al. or Bors et al., could not accomplish the principal of operation including supplying a bias to the wafer lifter during plasma processing as claimed and disclosed by Applicants.

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." *In re Ratti*, 270 F.2d 810, 123, USPQ 349 (CCPA 1959).

"If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

"A *prima facie* case of obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the claimed invention." *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997).

"A prior art reference must be considered in its entirety, i.e., as a whole including portions that would lead away from the claimed invention." *W.L. Gore & Associates, Inc., Garlock, Inc.*, 721 F.2d, 1540, 220 USPQ 303 (Fed Cir. 1983), *cert denied*, 469 U.S. 851 (1984).

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Examiner argues that regardless of the differences in the structure of Applicants disclosed and claimed invention and the combined teachings of Ishi et al. and Somekh et al. or Bors et al., that "a *prima facie* case of obviousness still exists because no unexpected results have been shown". Applicants respectfully suggest Examiner is mistaken in suggesting Applicants have a required showing of unexpected results.

The "unexpected results" analysis applies to processes involving claimed ranges (see MPEP 2131.03). Moreover, "unexpected results" are to be considered by the Examiner upon submission by the Applicants to overcome a *prima facie* case of obviousness (see MPEP 2144.05 (II) Overlapping ranges). A *prima facie* case of obviousness is not made out by Applicants failure to argue or show unexpected results.

2. Claim 9 stands rejected under 35 USC 103(a) as being unpatentable over Ishi et al., (US 5,571,366) in view of Somekh et al. (US 5,643,366) or Bors et al. (EP 0276061), as applied above, and further in view of Uchida (US 5,804,027) or Ishi et al. (US 5,795,429).

Applicants reiterate the comments made above with respect to Ishi et al., Somekh et al. or Bors et al.

In addition, even assuming *arguendo*, proper motivation for combination, the combination of the teachings of Ishi et al., with Somekh et al. or Bors et al., and further in view of Uchida or Ishi et al. '429, does not produce Applicants disclosed and claimed invention and does not help Examiner in making out a *prima facie* case of obviousness.

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Applicants point out that "we do not pick and choose among the individual elements of assorted prior art references to recreate the claimed invention, but rather we look for some teaching or suggestion in the references to support their use in a particular claimed combination" *Symbol Technologies, Inc. v. Opticon, Inc.*, 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991).

3. Claims 19 and 18 stand rejected under 35 USC 103(a) as being unpatentable over Ishi et al., (US 5,571,366) in view of Somekh et al. (US 5, 643, 366) or Bors et al. EP 0276061, as applied above, and further in view of Admitted Prior Art.

Applicants reiterate the comments made above with respect to Ishi et al., Somekh et al. or Bors et al.

Applicants further respectfully point out that Examiner is erroneously looking to Applicants disclosure for a suggestion to combine the teachings of references, i.e., as a roadmap to recreate Applicants disclosed and claimed invention.

"The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

In addition, even assuming *arguendo*, proper motivation for combination, the combination of Ishi et al. with Somekh et al. or

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Bors et al., and further in view of Applicants alleged admitted prior art, does not produce Applicants disclosed and claimed invention and does not help Examiner in making out a *prima facie* case of obviousness.

4. Claims 1, 3-5, 7-8, 10-13, and 15-19 stand rejected under 35 USC 103(a) as being unpatentable over Admitted Prior Art in view of Ishi et al., (US 5,571,366), and Somekh et al. (US 5, 643, 366) or Bors et al. (EP 0276061).

Applicants reiterate the comments made above with respect to Applicants alleged admitted prior art, Ishi et al., and Somekh et al. or Bors et al.

In addition, even assuming *arguendo*, proper motivation for combination, the combination of Applicants alleged admitted prior with and Ishi et al., Somekh et al. or Bors et al., does not produce Applicants disclosed and claimed invention and does not help Examiner in making out a *prima facie* case of obviousness.

Applicants again point out that "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

5. Claim 9 stands rejected under 35 USC 103(a) as being unpatentable over Admitted prior art in view of Ishi et al. (US 5,571,366), and Somekh et al. (US 5, 643, 366) or Bors et al. EP 0276061, as applied *above*, and further in view of Uchida (US 5,804,027) or Ishi et al. (US 5,795,429).

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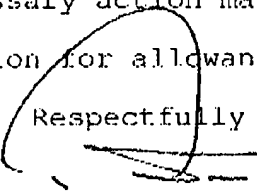
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Applicants reiterate the comments made above with respect to Applicants alleged admitted prior art, Ishi et al., and Somekh et al. or Bors et al.

In addition, even assuming *arguendo*, proper motivation for combination, the combination of Applicants alleged admitted prior with and Ishi et al., and Somekh et al. or Bors et al., and further in view of Uchida or Ishi et al. '429, does not produce Applicants disclosed and claimed invention and does not help Examiner in making out a *prima facie* case of obviousness.

Applicants have amended their claims to clarify their invention, adding no new matter, or raising no new issues, but rather incorporating previously presented limitations from the dependent claims into the independent claims. Based on the foregoing, the Applicants respectfully submit that the claims are now in condition for allowance, and request Examiner to reconsider and withdraw final rejection and allow the claims as presented. Such favorable action by the Examiner at an early date is respectfully solicited. In the event that the present invention is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,


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